Low Charge Injection 16-Channel High Voltage Analog Switch

Features

- HVCMOS technology for high performance
- 16-channel high voltage analog switch
- 3.3V input logic level compatible
- 20MHz data shift clock frequency
- Very low quiescent power dissipation (-10µA)
- Low parasitic capacitance
- DC to 50MHz small signal frequency response
- -60dB typical OFF-isolation at 5.0MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Cascadable serial data register with latches
- Flexible operating supply voltages

Applications

- Medical ultrasound imaging
- NDT metal flaw detection
- Piezoelectric transducer drivers
- Optical MEMS modules

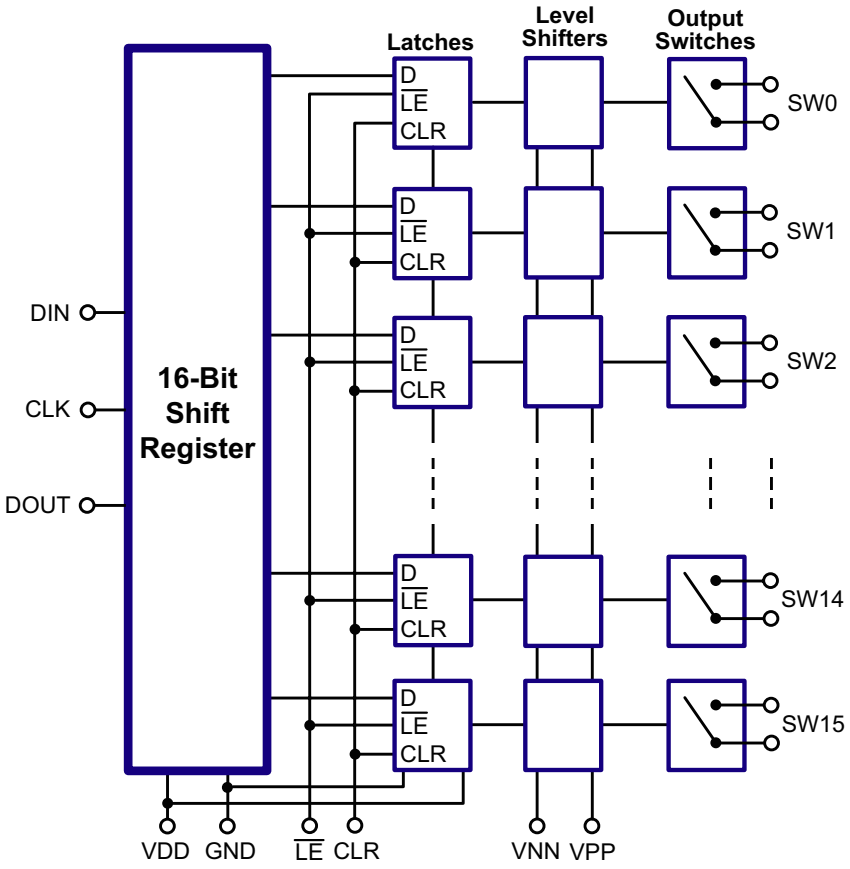
General Description

The Supertex HV2601 is a low charge injection 16-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers.

Input data are shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN}: +40V/-160V, +100V/-100V, and +160V/-40V.

Block Diagram



Ordering Information

Device	Package Options		
	42-Ball Bumped Die *5.29x5.30mm body* *1.01mm height (max)* *0.52 / 0.60mm pitch*	48-Lead LQFP *7.00x7.00mm body* *1.60mm height (max)* *0.50mm pitch*	48-Ball fpBGA *7.00x8.00mm body* *1.16mm height (max)* *0.75mm pitch*
HV2601	HV2601BD M936	HV2601FG-G	HV2601GA-G

-G indicates package is RoHS compliant ('Green').
Bumped Die package is RoHS compliant ('Green').
M936 specifies product in tape and reel.

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP} - V_{NN} differential supply	220V
V_{PP} positive supply	-0.5V to V_{NN}+200V
V_{NN} negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V_{DD} +0.3V
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation: 42-Ball Bumped Die (BD) 48-Lead LQFP (FG) 48-Ball fpBGA (GA)	 1.5W 1.0W 1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

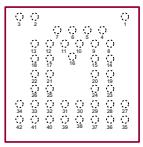
Recommended Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage	3.0V to 5.5V
V_{PP}	Positive high voltage supply	+40V to V_{NN} +200V
V_{NN}	Negative high voltage supply	-40V to -160V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
V_{SIG}	Analog signal voltage peak-to-peak	V_{NN}+10V to V_{PP}-10V
T_A	Operating free air temperature	0°C to 70°C

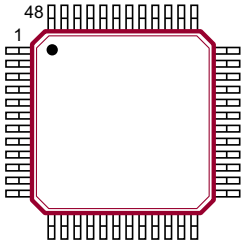
Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *V_{SIG} must be within V_{NN} and V_{PP} or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{PP} and V_{NN} should not be less than 1.0msec.*

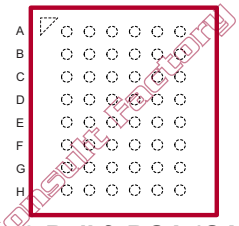
Pin Configurations



42-Ball Bumped Die (BD)
(top view)



48-Lead LQFP (FG)
(top view)



48-Ball fpBGA (GA)
(top view)

Product Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number

Package may or may not include the following marks: Si or

42-Ball Bumped Die (BD)

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

48-Lead LQFP (FG)

YY = Year Sealed
WW = Week Sealed
L = Lot Number
_____ = "Green" Packaging

48-Ball fpBGA (GA)

Packages may or may not include the following marks: Si or

DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS}	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I_{SIG} = 5.0mA	V_{PP} = +40V, V_{NN} = -160V
		-	25	-	22	27	-	32		I_{SIG} = 200mA	
		-	25	-	22	27	-	30		I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = -100V
		-	18	-	18	24	-	27		I_{SIG} = 200mA	
		-	23	-	20	25	-	30		I_{SIG} = 5.0mA	V_{PP} = +160V, V_{NN} = -40V
		-	22	-	16	25	-	27		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = -100V	
R_{ONL}	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V_{SIG}=V_{PP} - 10V, I_{SIG} = 1.0A	
I_{SOL}	Switch OFF leakage per switch*	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} - 10V and V_{NN} + 10V	
V_{OS}	DC offset switch OFF*	-	300	-	100	300	-	300	mV	100kΩ load	
	DC offset switch ON*	-	500	-	100	500	-	500	mV		
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches OFF	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches OFF	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-10	-50	-	-	µA	All switches ON, I_{SW} = 5.0mA	
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load.
		-	4.0	-	-	5.5	-	5.5		V_{PP} = +100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V, V_{NN} = -40V	
I_{NN}	Average V_{NN} supply current	-	6.5	-	-	7.0	-	8.0	mA	V_{PP} = +40V, V_{NN} = -160V	All output switches are turning ON and OFF at 50kHz with no load.
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +100V, V_{NN} = -100V	
		-	4.0	-	-	5.0	-	5.5		V_{PP} = +160V, V_{NN}=-40V	
I_{DD}	Average V_{DD} supply current	-	4.0	-	-	4.0	-	4.0	mA	f_{CLK} = 5.0MHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static	
I_{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = V_{DD} -0.7V	
I_{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V_{OUT} = 0.7V	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

** See Test Circuits on page 5*

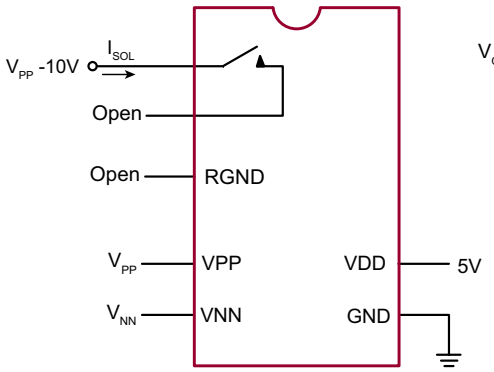
AC Electrical Characteristics

(over recommended operating conditions, V_{DD}= 5.0V, t_R= t_F≤ 5ns, 50% duty cycle, C_{LOAD}= 20pF unless otherwise noted)

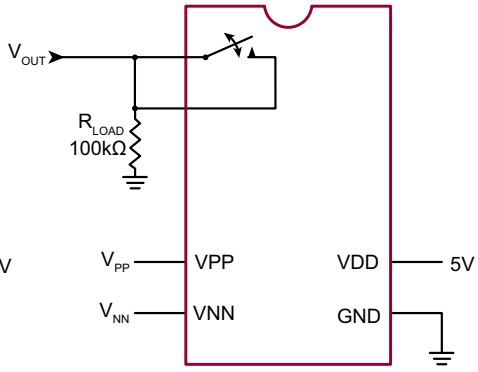
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
t_{WLE}	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	V_{DD} = 3.0V
		12	-	-	12	-	12	-		V_{DD} = 5.0V
t_{DO}	Clock delay time to data out	50	100	50	78	100	50	100	ns	V_{DD} = 3.0V
		15	40	15	30	40	15	40		V_{DD}= 5.0V
t_{WCLR}	Time width of CLR	55	-	55	-	-	55	-	ns	---
t_{SU}	Set up time data to clock	21	-	-	21	-	21	-	ns	V_{DD}= 3.0V
		7	-	-	7	-	7	-		V_{DD}= 5.0V
t_H	Hold time data from clock	2	-	2	-	-	2	-	ns	V_{DD}= 3.0 or 5.0V
f_{CLK}	Clock frequency	-	8	-	-	8	-	8	MHz	V_{DD}= 3.0V
		-	20	-	-	20	-	20		V_{DD}= 5.0V
t_R,t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
T_{ON}	Turn ON time*	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10kΩ
T_{OFF}	Turn OFF time*	-	5.0	-	-	5.0	-	5.0	µs	V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10kΩ
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	v/ns	V_{PP} = +40V, V_{NN} = -160V
		-	20	-	-	20	-	20		V_{PP} = +100V, V_{NN} = -100V
		-	20	-	-	20	-	20		V_{PP} = +160V, V_{NN} = -40V
K_O	OFF isolation*	-30	-	-30	-33	-	-30	-	dB	f = 5.0MHz, 1kΩ//15pF load
		-58	-	-58	-	-	-58	-		f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk*	-60	-	-60	-70	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	300	-	-	300		300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	ON capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, f = 1.0MHz
$+V_{SPK}$	Output voltage spike*	-	-	-	-	150	-	-	mV	V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50Ω
$-V_{SPK}$										
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50Ω
$-V_{SPK}$										
$+V_{SPK}$		-	-	-	-	150	-	-		V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50Ω
$-V_{SPK}$										
QC	Charge injection*	-	-	-	820	-	-	-	pC	V_{PP}= +40V, V_{NN}= -160V, V_{SIG}= 0V
		-	-	-	600	-	-	-		V_{PP}= +100V, V_{NN}= -100V, V_{SIG}= 0V
		-	-	-	350	-	-	-		V_{PP}= +160V, V_{NN}= -40V, V_{SIG}= 0V

** See Test Circuits on page 5*

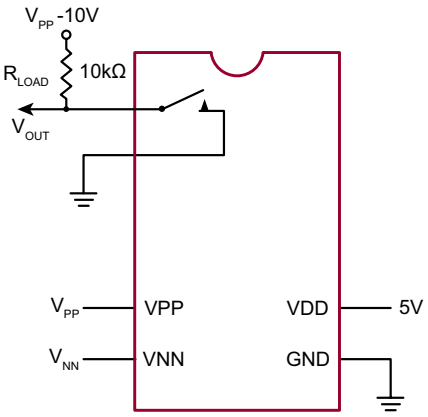
Test Circuits



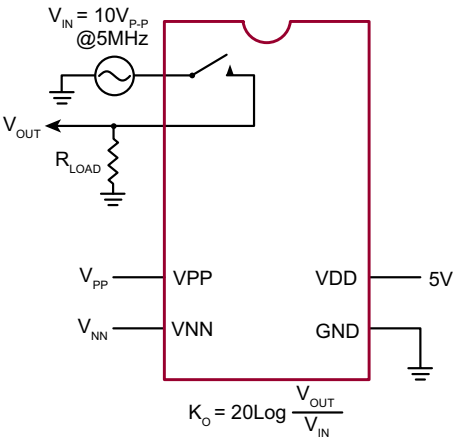
Switch Off Leakage per Switch



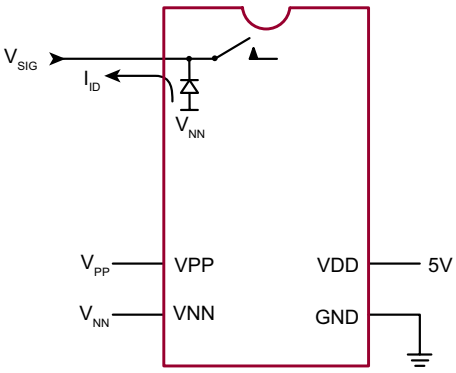
DC Offset Switch ON/OFF



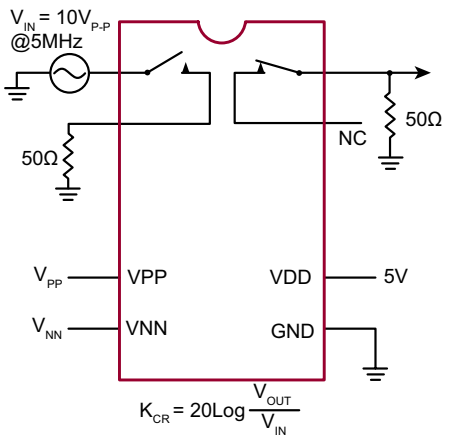
T_{ON}/T_{OFF} Test Circuit



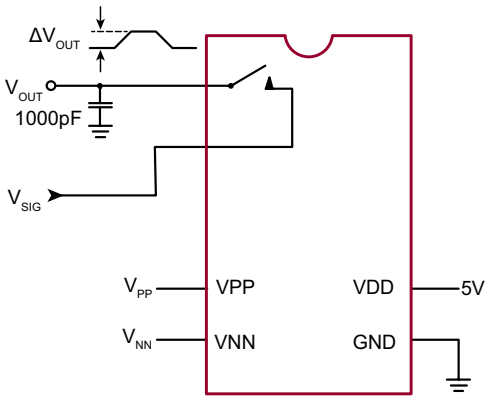
OFF Isolation



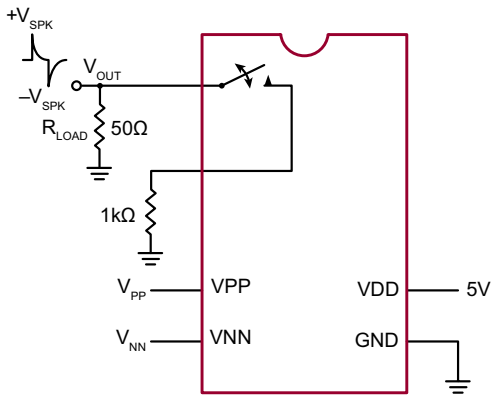
Output Switch Isolation Diode Current



Switch Crosstalk



$Q = 1000pF \times \Delta V_{OUT}$ Charge Injection



Output Voltage Spike

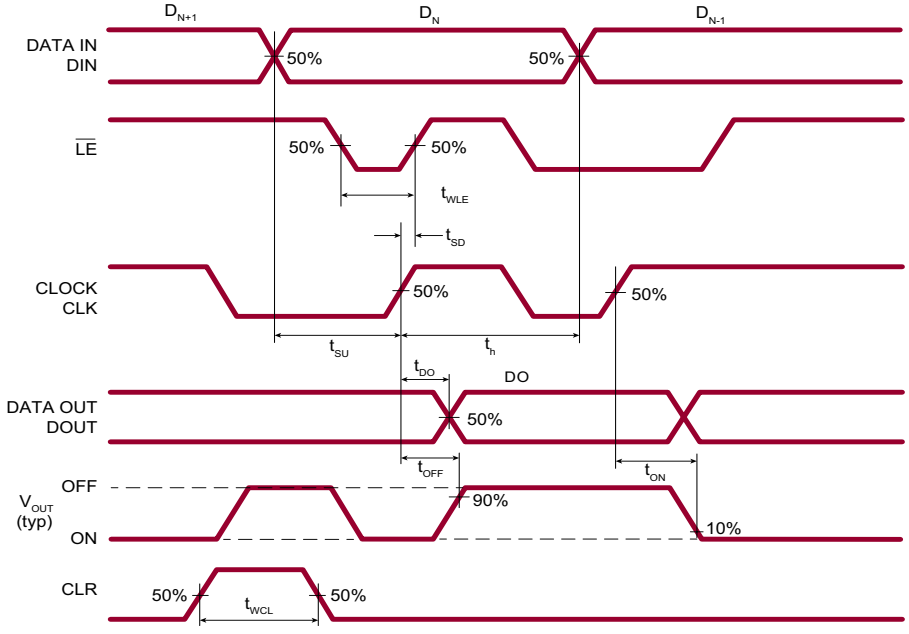
Logic Function Table

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		OFF	-		-
-	-		L	-		-	L	L	-	-		ON	-		-
-	-		H	-		-	L	L	-	-		-	OFF		-
-	-	...	-	L	...	-	L	L	-	-	...	-	ON	...	-
-	-		-	H		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. *The 16 switches operate independently.*
2. *Serial data is clocked in on the L to H transition of the CLK.*
3. *All 16 switches go to a state retaining their latched condition at the rising edge of $\overline{LE}$. When $\overline{LE}$ is low the shift registers data flow through the latch.*
4. *D_{OUT} is high when data in the shift register 15 is high.*
5. *Shift registers clocking has no effect on the switch states if $\overline{LE}$ is high.*
6. *The CLR clear input overrides all other inputs.*

Logic Timing Waveforms



Ball Description
42-Ball Bumped Die Package Outline (BD)

Ball #	Ball Name	Ball Coordinates*	
		X	Y
1	NC	+2100.00	-2239.50
2	VPP	-1500.00	-2239.50
3	VNN	-2100.00	-2239.50
4	DOUT	+1200.00	-1719.75
5	CLR	+600.00	-1719.75
6	CLK	0.00	-1719.75
7	GND	-600.00	-1719.75
8	SW15A	+1500.00	-1200.00
9	SW15B	+900.00	-1200.00
10	$\overline{\text{LE}}$	+300.00	-1200.00
11	VDD	-300.00	-1200.00
12	SW0A	-900.00	-1200.00
13	SW0B	-1500.00	-1200.00
14	SW14A	+1500.00	-600.00
15	SW14B	+900.00	-600.00
16	DIN	0.00	-680.25
17	SW1A	-900.00	-600.00
18	SW1B	-1500.00	-600.00
19	SW13A	+1500.00	0.00
20	SW13B	+900.00	0.00
21	SW2A	-900.00	0.00

Ball #	Ball Name	Ball Coordinates*	
		X	Y
22	SW2B	-1500.00	0.00
23	SW12A	+1500.00	+600.00
24	SW12B	+900.00	+600.00
25	SW3A	-900.00	+600.00
26	SW3B	-1500.00	+600.00
27	SW11A	+2100.00	+1200.00
28	SW11B	+1500.00	+1200.00
29	SW9B	+900.00	+1200.00
30	SW8B	+300.00	+1200.00
31	SW7A	-300.00	+1200.00
32	SW6A	-900.00	+1200.00
33	SW4A	-1500.00	+1200.00
34	SW4B	-2100.00	+1200.00
35	SW10B	+2100.00	+1800.00
36	SW10A	+1500.00	+1800.00
37	SW9A	+900.00	+1800.00
38	SW8A	+300.00	+1800.00
39	SW7B	-300.00	+1800.00
40	SW6B	-900.00	+1800.00
41	SW5B	-1500.00	+1800.00
42	SW5A	-2100.00	+1800.00

Note:

** Referenced from center of package (µm).*

Pin Description
48-Lead LQFP (FG)

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	NC	13	VNN	25	SW15B	37	SW10B
2	NC	14	NC	26	SW15A	38	SW10A
3	SW4B	15	VPP	27	SW14B	39	SW9B
4	SW4A	16	NC	28	SW14A	40	SW9A
5	SW3B	17	GND	29	SW13B	41	SW8B
6	SW3A	18	VDD	30	SW13A	42	SW8A
7	SW2B	19	DIN	31	SW12B	43	SW7B
8	SW2A	20	CLK	32	SW12A	44	SW7A
9	SW1B	21	$\overline{LE}$	33	SW11B	45	SW6B
10	SW1A	22	CLR	34	SW11A	46	SW6A
11	SW0B	23	DOUT	35	NC	47	SW5B
12	SW0A	24	NC	36	NC	48	SW5A

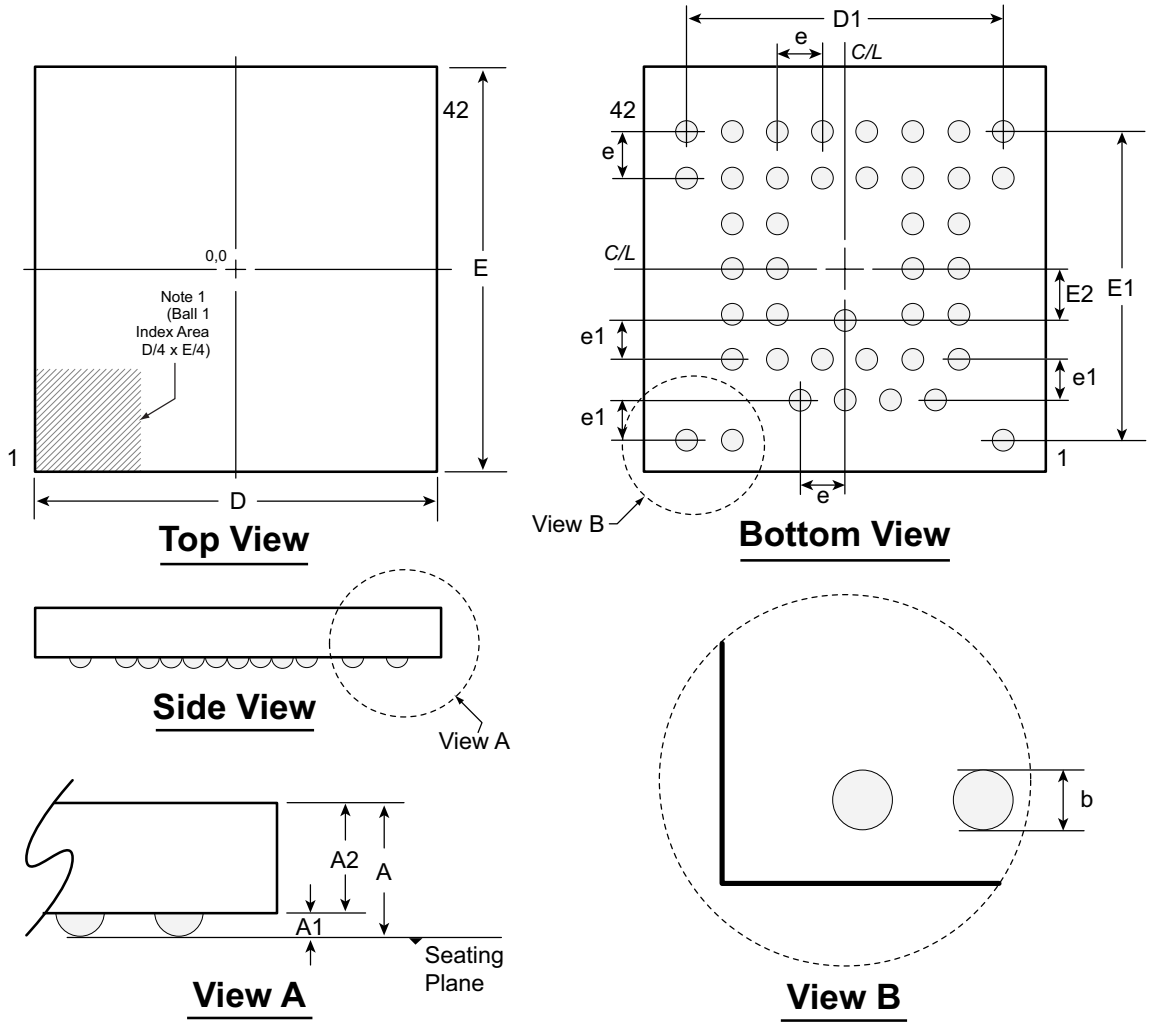
Pin Configuration
48-Ball fpBGA (GA)

Ball #	Function	Ball #	Function	Ball #	Function	Ball #	Function
A1	SW5A	C1	SW4B	E1	SW1B	G1	NC
A2	SW5B	C2	SW3B	E2	SW0B	G2	GND
A3	SW7A	C3	SW2B	E3	SW15B	G3	NC
A4	SW7B	C4	SW13A	E4	SW15A	G4	DIN
A5	SW9A	C5	SW12A	E5	SW14B	G5	CLK
A6	SW9B	C6	SW11A	E6	SW14A	G6	DOUT
B1	SW6A	D1	SW4A	F1	SW1A	H1	VNN
B2	SW6B	D2	SW3A	F2	SW0A	H2	NC
B3	SW8A	D3	SW2A	F3	NC	H3	VPP
B4	SW8B	D4	SW13B	F4	NC	H4	NC
B5	SW10A	D5	SW12B	F5	VDD	H5	$\overline{LE}$
B6	SW10B	D6	SW11B	F6	NC	H6	CLR

NC = No Internal Connection

42-Ball Bumped Die Package Outline (BD)

5.29x5.30mm body, 1.01mm height (max), 0.52 / 0.60mm pitch



Notes:

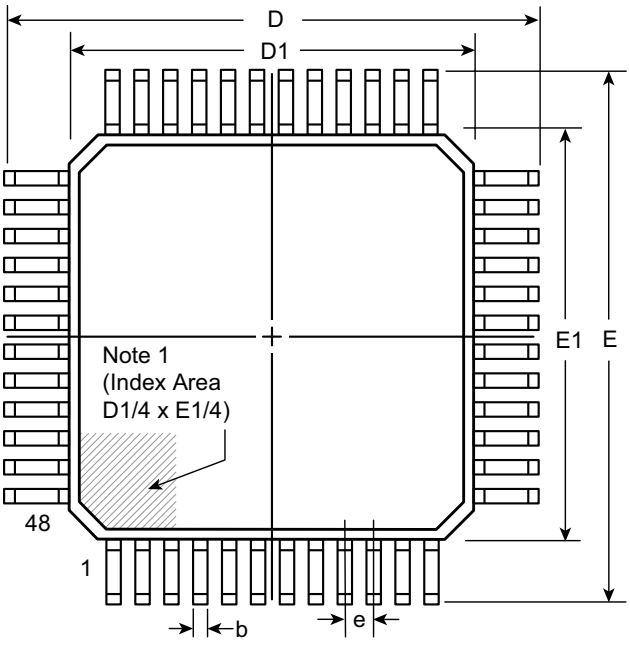
1. *Ball 1 identifier must be located in the index area indicated. Ball 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	e1
Dimension (mm)	MIN	0.89	0.21	0.68	0.29	5.19	4.20 BSC	5.20	4.04 BSC	0.68 BSC	0.60 BSC	0.52 BSC
	NOM	0.95	0.24	0.71	0.32	5.29		5.30				
	MAX	1.01	0.27	0.74	0.35	5.39		5.40				

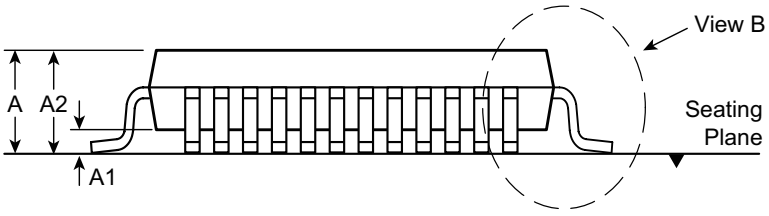
Drawings not to scale.
Supertex Doc. #: *DSPD-42BumpedDieBD, Version A030211.*

48-Lead LQFP Package Outline (FG)

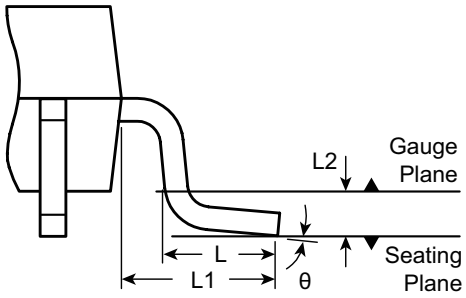
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



Side View



View B

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

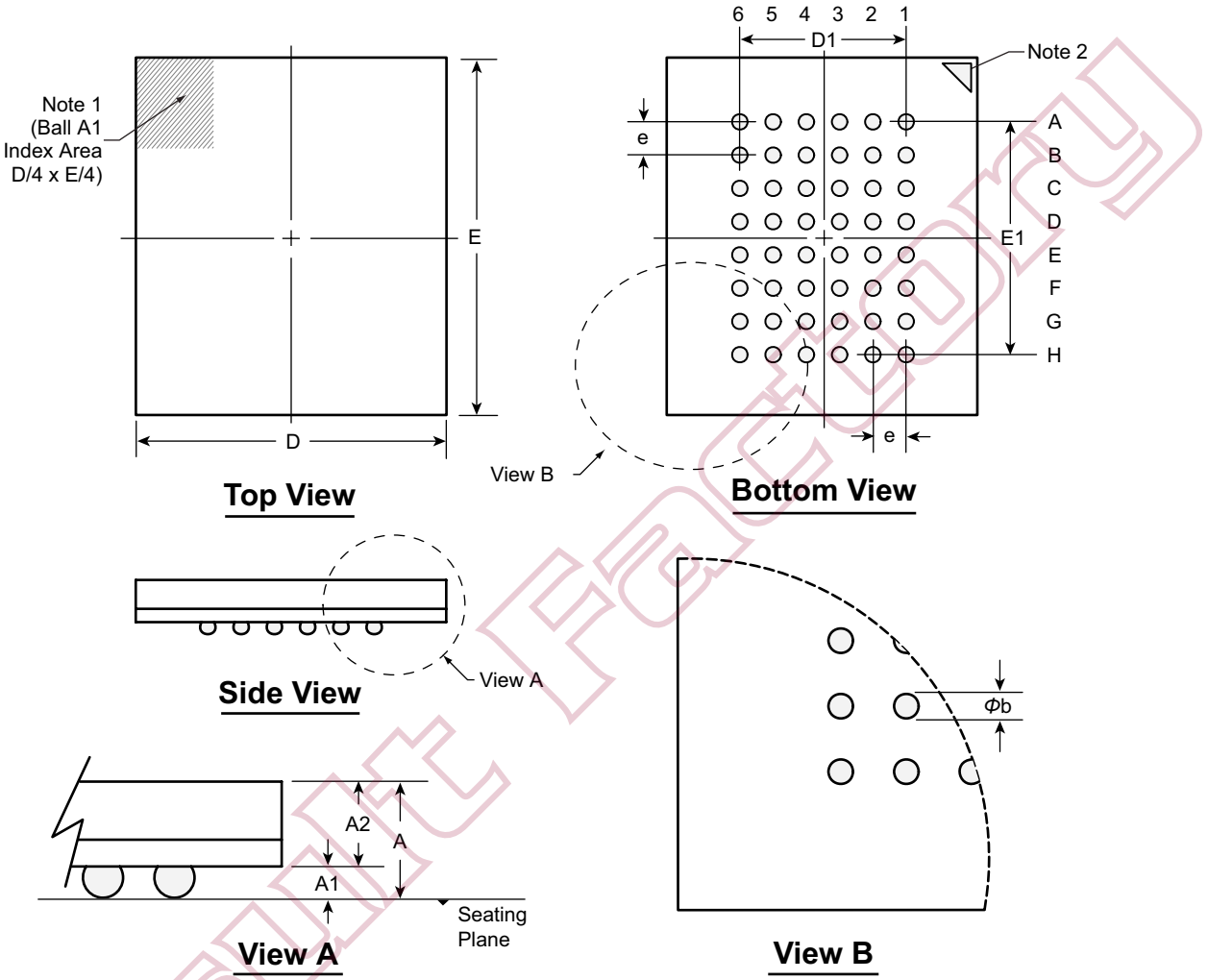
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

***Supertex Doc. #:** DSPD-48LQFPFG Version, D041309.*

48-Ball fpBGA Package Outline (GA)

7.00x8.00mm body, 1.16mm height (max), 0.75mm pitch



Notes:

1. *Ball A1 identifier must be located in the index area indicated. Ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*
2. *Corner A1 identifier (actual shape may vary).*

Symbol		A	A1	A2	b	D	D1	E	E1	e
Dimension (mm)	MIN	0.86	0.18	0.68	0.25	6.90	3.75 BSC	7.90	5.25 BSC	0.75 BSC
	NOM	1.01	0.23	0.78	0.30	7.00		8.00		
	MAX	1.16	0.28	0.88	0.35	7.10		8.10		

Drawings not to scale.
Supertex Doc. #: *DSPD-48fpBGAGA, Version C020309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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